REMARKS

This is in full and timely response the Office Action mailed on September 13, 2004. Reexamination in light of the following remarks is respectfully requested.

Claims 13-25 are currently pending in this application, with claim 13 being independent. *No new matter has been added.*

Prematureness

Applicant, seeking review of the ***prematureness*** of the final rejection within the Final Office Action, respectfully requests reconsideration of the finality of the Office Action for the reasons set forth hereinbelow. See M.P.E.P. §706.07(c).

If the allowance of the claim is not forthcoming at the very least and a new ground of rejection made, then a ***new non-final Office Action*** is respectfully requested, at least for the following reasons.

Drawing objections

In response to the objection to the drawings, drawings have been provided on May 20, 2004 that include figures 1 and 2 having a legend such as -- Related Art --. This legend is consistent with the specification as originally filed, in which figures 1 and 2 are described in the section titled "Description of the Related Art". Also note that no requirement for the specific use of "Prior Art" as a legend is found within 37 C.F.R. §1.84.

Nevertheless, while not conceding the propriety of this objection and in order to advance the prosecution of the above-identified application, figures 1 and 2 having a legend such as -- Prior

Art -- have been provided within the Request For Approval Of Drawing Corrections filed along with this Reply.

Withdrawal of this objection is respectfully requested.

Rejections under 35 U.S.C. §103

Claims 13-25 were rejected under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 5,454,100 to Sagane in view of U.S. Patent No. 5,701,506 to Hosotani.

This rejection is respectfully traversed at least for the following reasons.

As an initial matter, the Office Action fails to identify with particularity the elements of Sagane and Hosotani that are to be associated with the features of the claimed invention. Thus, this rejection is vague at best by lacking clarity and completeness.

"The Patent and Trademark Office (PTO) has the burden of showing a prima facie case of obviousness." *In re Bell*, 26 USPQ2d 1529, 1530 (Fed. Cir. 1993). "In determining the propriety of the Patent Office case for prima facie obviousness, it is necessary to ascertain whether the prior art teachings would appear to be sufficient to one of ordinary skill in the art to suggest making the proposed substitution or other modification." *In re Taborsky*, 183 USPQ 50, 55 (CCPA 1974). Moreover, *prima facie* obviousness of a claimed invention is established "only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references." *In re Fine*, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).

Claim 13 and the claims dependent thereon include the features of:

a debugging circuit having a plurality of bug address setting registers and a plurality of coincidence detecting circuits,

one of said plurality of bug address setting registers holding one of a plurality of bug addresses that show the start of a buggy part of said program stored in said program memory,

one of said plurality of coincidence detecting circuits comparing a program address for reading instruction codes from said program memory with said one of said plurality of bug addresses held in said one of said plurality of bug address setting registers, said one of said plurality of coincidence detecting circuits outputting one of a plurality of coincidence signals when said program address and said one of said plurality of bug addresses coincide,

another of said plurality of bug address setting registers holding another of said plurality of bug addresses that show the start of another buggy part of the program stored in the program memory,

another of said plurality of coincidence detecting circuits comparing said program address for reading instruction codes from said program memory with said another of said plurality of bug addresses held in said another of said plurality of bug address setting registers, said another of said plurality of coincidence detecting circuits outputting another of said plurality of coincidence signals when said program address and said another of said plurality of bug addresses coincide; and

a central processing unit receiving said plurality of coincidence signals, wherein said central processing unit:

executes one of a plurality of debugging programs stored within random access memory when said one of said plurality of coincidence signals indicates a coincidence of said program address and said one of said plurality of bug addresses,

executes another of said plurality of debugging programs stored within said random access memory when said another of said plurality of coincidence signals indicates a

coincidence of said program address and said another of said plurality of bug addresses, and

executes said program stored within said program memory when said plurality of coincidence signals indicates a non-coincidence of said program address and any of said plurality of bug addresses.

Sagane arguably teaches an electronic apparatus. Figure 1 is a block diagram of the *first embodiment* while figure 3 of Sagane is a block diagram of the *second embodiment* of the invention.

The Office Action refers to column 6, lines 7-9 of Sagane, which is part of the description for the *second embodiment*. The Office Action also refers to column 3, lines 32-34 and lines 48-52 of Sagane, which are part of the description for the *first embodiment*. The Office Action identifies column 6, lines 41-52 and 37-40 and column 6, line 67 to column 7, line 3, of Sagane, which are part of the description for the *second embodiment*, and column 3, lines 48-52, which are part of the description for the *first embodiment*.

In this regard, there is considerable confusion within the Office Action regarding the particular embodiment within Sagane upon which the rejection of the claims is based.

Regarding the first embodiment of Sagane, if the ROM 3 includes a plurality of bugs to be corrected, Sagane arguably teaches that step S10 of figure 2 may be followed for each bug by a step of updating the interrupt generating address register 9 and the interrupt vector register 7b to reflect the next correction address and the start address of the next correction content, respectively (Sagane at figure 1, column 5, lines 49-54).

Yet, the Office Action fails to show within the first embodiment of Sagane where the feature of a debugging circuit having a plurality of bug address setting registers and a plurality of coincidence detecting circuits is found (Sagane at figure 1).

Regarding the second embodiment, Sagane arguably teaches that step S31 of figure 4 may be followed for each bug by a step of updating the correction address register 21 and the correction data register 22 to reflect the next correction address and the next correction data, respectively (Sagane at column 6, lines 63-67).

However, the Office Action fails to disclose, teach or suggest how this feature of Sagane results in a debugging circuit having a plurality of bug address setting registers and a plurality of coincidence detecting circuits.

While figure 3 of Sagane arguably teaches a single central processing unit 2, a single comparator 8, a single correction address register 21 and a single correction data register 22, Sagane arguably teaches that a pluralities of comparators 8, correction address registers 21 and correction data registers 22 may be provided to address the multiple bugs (Sagane at figure 3, column 7, lines 1-3). But note that figure 3 of Sagane is a block diagram of the *second embodiment* of the invention. Whereas like reference characters designate like or corresponding parts (Sagane at column 6, lines 3-6), a correction address register 21 and a correction data register 22 depicted within figure 3 are not found within figure 1, and an access switching unit 7 depicted within figure 1 is not found within figure 3.

Regarding the assertion on page 5 of the Office Action that Sagane depicts CPU 2 in figure 1 as receiving a plurality of coincidence signals, please note that figure 1 of Sagane arguably depicts a comparator 8 that supplies the interrupt control circuit 7d with a coincidence signal E via the switch 7c, thereby generating an interrupt (Sagane at column 5, lines 13-17). However, the Office Action fails to show where and how the CPU 2 of figure 1 is to receive a plurality of coincidence signals.

Regarding the assertion on page 5 of the Office Action that Sagane depicts CPU 2 in figure 3 as receiving a plurality of coincidence signals, please note that the Office Action fails to clearly identify in figure 3 of Sagane where and how the CPU 2 is to receive a plurality of

coincidence signals, since signal A of comparator 8 found within figure 3 is applied to switch 23 and not to CPU 2.

Note additionally, page 5 of the Office Action asserts that Sagane ***depicts*** *CPU 2 in figures 1 and 3 receiving* a plurality of coincidence signals, whereas page 6 of the Office Action asserts that Sagane ***does not expressly disclose*** *the central processing unit receiving* a plurality of coincidence signals. These assertions are in clear contradiction, rendering the Office Action vague and indefinite at best.

Thus, the Office Action fails to disclose, teach or suggest either figure 1 of Sagane for the first embodiment or figure 3 for the second embodiment as depicting a central processing unit 2 that receives a plurality of coincidence signals.

The Office Action cites Hosotani for the features deficient within Sagane. Hosotani arguably teaches microcomputer having ROM program that can be altered. Within Hosotani the first to third match circuits 9a-9c are connected to a three-input OR circuit 14. Hosotani arguably teaches that the output of OR circuit 14 is applied to switch 10 (Hosotani at figures 2, 6, 8, 10, 11) or to ROM 17 (Hosotani at figures 7, 12). Yet, Hosotani fails to disclose, teach or suggest the output of OR circuit 14 being applied to CPU 1.

Sagane and Hosotani, either individually or as a whole, fail to disclose, teach or suggest the features found within the claimed invention. Withdrawal of this rejection and allowance of the claims is respectfully requested.

Conclusion

For the foregoing reasons, all the claims now pending in the present application are allowable, and the present application is in condition for allowance. Accordingly, favorable reexamination and reconsideration of the application in light of the remarks is courteously solicited.

If the Examiner has any comments or suggestions that could place this application in even better form, the Examiner is requested to telephone Brian K. Dutton, Reg. No. 47,255, at 202-955-8753 or the undersigned attorney at the below-listed number.

If any fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

Dated: October 29, 2004

Respectfully submitted,

By_____

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